Applicant has amended claims 1, 3, 5, 8, 10 and 15. Claims 1-16 are pending in this application.

The Examiner objected to claims 5-7 and 12-14 under 37 C.F.R. Section 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. Applicant believes that the multiple dependency problem was resolved with the filing of a Preliminary Amendment dated January 18, 2005. Accordingly, applicant respectfully requests withdrawal of the objection to claims 5-7 and 12-14.

The Examiner rejected claims 3 and 10 under 35 U.S.C. Section 112, second paragraph as being indefinite. Applicant has amended claims 3 and 10 to delete the phrase "relatively high value" from both claims 3 and 10.

The Examiner rejected claims 1-16 under 35 U.S.C. Section 102(b) as being anticipated by Matsuda (US Patent No. 4,709,341). Applicant respectfully traverses the rejection.

Matsuda describes a self-monitoring system in which the outputs of one or more processors are checked by either the issuing processor or another processor in the system to ensure that the microprocessors are operating correctly. As shown in FIG. 3, for example, output voltage signals from P10 and P11 of the microprocessor serve as inputs to ports P20 and P21 of the processor. These ports P20, P21 are check ports. The voltage level at the check port P20 is indicative of the output level of the output port P10 of the microprocessor (col. 4, lines 16-18).

In all embodiments described, it is the output of the processor that is checked and not the operation of the load itself. That means that any error that occurs downstream of the outputs of the processors are not detected by the self-monitoring system of Matsuda. Therefore, the Matsuda system would report no fault even if there was a fault downstream.

By contrast, in the present invention as shown by FIG. 1, for example, the second microprocessor 18 monitors the operation of the first microprocessor 16 as well as the load 10 itself (see paragraph 11 of the published application). In FIG. 1, the voltage output of the processor 16 is checked by the processor 18 through R1 and the operation of the load 10 is monitored by the processor 18 through the input line from point A to the processor 18. Thus, the present invention provides the advantage that any error in the system that causes the load to operate in an unexpected way is detectable by the processor and the load is switched off as a consequence. This provides a fail-safe system which is lacking in known systems such as Matsuda.

This feature is recited in claim 1 as "when either microprocessor *detects a fault in the control of the load* the load is switched off" (emphasis added). However, solely to clarify that feature and

not to limit the claim in any way, claim 1 has been amended to recite "a second microprocessor . . . . being arranged to monitor the operation of the load".

Applicant respectfully submits that Matsuda fails to teach or suggest the novel feature of a microprocessor monitoring the operation of the load.

Independent claim 8 has been amended similarly to claim 1. Independent claim 15 recites "a second microprocessor to monitor . . . the operation of the load". Independent claim 16 recites "monitoring the . . . operation of the load by means of a second microprocessor". For the similar reasons as discussed above with respect to claim 1, applicant submits that independent claims 8, 15 and 16 are also patentable over the Matsuda reference.

Dependent claims 2-7 and 9-14 are also patentable by virtue of their dependency from independent claims 1 or 8.

Based upon the above amendments and remarks, Applicant respectfully requests reconsideration of this application and its earlier allowance. Should the Examiner feel that a telephone conference with Applicant's attorney would expedite the prosecution of this application, the Examiner is urged to contact him at the number indicated below.

Respectfully submitted,

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